JAPANESE PATENT OFFICE

PATENT JOURNAL

KOKAI PATENT APPLICATION NO. HEI 5[1993]-129517

Technical Disclosure Section

Int. Cl.[5]:	H 01 L 25/065 25/07 25/18 21/60 H 01 L 25/08
Sequence Nos. for Office Use:	6918-4M 7220-4M
Application No.:	Hei 4[1992]-114940
Application Date:	May 7, 1992
Publication Date:	May 25, 1993
No. of Claims:	14 (Total of 7 pages)
Priority	
Date:	May 11, 1991
Country:	Korea
No.:	1991P7632
Examination Request:	Requested

A LAMINATED SEMICONDUCTOR PACKAGE AND ITS MANUFACTURING METHOD

Inventor: Wen Senkou
554-17 Kousoudou,
Jyouhoku-ku,
Soul Tokubetsu-shi,
Daikanminkoku

Applicant: 591050992
Kaneboshi Electron K.K.
50 Kouteidou,
Cushinhokudou
seishu-shi,
Daikanminkoku

Agent: Kou Asamura,
patent attorney,
and 3 others

[There are no amendments to this patent.]

Abstract

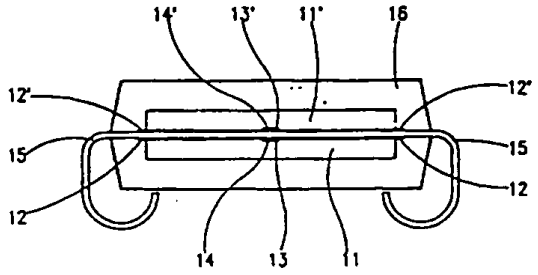
Objective

[The present invention] offers a laminated semiconductor package and its manufacturing method, in which each of the inner leads is bonded to the upper and lower side semiconductor chips by soldering in order to improve the integration and to obtain a thin element.

Constitution

A laminated semiconductor package manufacturing method is offered, in which polyimide is formed at the surface of one side of upper and lower side semiconductor chips, a solder is

respectively formed at each pad of said upper and lower side semiconductor chips, each of the inner leads is lined up with these solders, these inner leads are then bonded to the semiconductor chips in a reflow furnace, and the upper and lower side semiconductor chips are bonded together through the application of encapsulating epoxy.



Claims

1. A laminated semiconductor package structured so that a thin element can be obtained, in which pads (13') and (13) are respectively formed over upper and lower side semiconductor chips (11') and (11), solders (14') and (14) are respectively formed over these pads (13') and (13), and inner leads (15) and (15) of a lead frame are respectively bonded to the aforementioned upper and lower side semiconductor chips (11') and (11) by these solders (14') and (14).

2. The laminated semiconductor package described in Claim 1, in which each of the aforementioned solders (14') and (14) is respectively formed from a Pb-Sn alloy.

3. The laminated type semiconductor package described in Claim 1 or 2, in which each of the aforementioned solders (14') and (14) is respectively formed into a ball shape.

4. The laminated semiconductor package described in Claim 1, in which each of the pads (13') and (13) of the aforementioned upper and lower side semiconductor chips (11') and (11) are respectively formed over the said chips (11') and (11) in 1 straight line in a condition in which each of said chips (11') and (11) is laminated, and each of the aforementioned solders (14') and (14) are respectively formed over said pads (13') and (13).

5. The laminated semiconductor package described in Claim 4, in which each of the pads (13') and (13) of the aforementioned upper and lower side semiconductor chips (11') and (11) is formed in 1 line in a manner such that they meet.

6. The laminated semiconductor package described in Claim 1, in which each of the pads (13') and (13) of the aforementioned upper and lower side semiconductor chips (11') and (11) is formed over said chips (11') and (11) in a manner so that they form 2 lines in a condition in which said chips (11') and (11) are laminated, and each of the solders (14') and (14) is respectively formed over said pads (13') and (13).

7. The laminated semiconductor package described in Claim 6 in which each of the aforementioned pads (13) and (13') is formed in 2 lines in a manner such that they meet.

8. The laminated semiconductor package described in Claim 6, in which each of the aforementioned pads (13) and (13') is formed in 2 lines in parallel, and each of the solders (14) and (14') is respectively formed over said pads (13) and (13').

9. The laminated semiconductor package described in Claim 4 or 6, in which at least 2 or more common pads (17) are included in each of the aforementioned pads (14) and (14').

10. A laminated semiconductor package manufacturing method consists of stage S1, in which polyimide [layers](12) and (12') are respectively formed at the surface of one side of both upper and lower side semiconductor chips (11) and (11'),

stage S2, in which each of the solders (14) and (14') are formed respectively over each of the pads (13) and (13') of the aforementioned upper and lower side semiconductor chips (11) and (11'),

stage S3, in which the edge of one side of each of the inner leads (15) and (15) is lined up with said solders (14) and (14'), and these inner leads (15) and (15') are respectively bonded to the aforementioned upper and lower side semiconductor chips (11) and (11'),

and stage S4, in which the upper side semiconductor chip (11'), to which each of the aforementioned S1, S2, and S3 stages is processed, is overturned and mounted over the lower side semiconductor chip (11), and the upper and lower side semiconductor chips (11) and (11') are bonded together through the application of an encapsulating resin.

11. The laminated semiconductor package manufacturing method described in Claim 10, in which, at the stage in which the aforementioned solders (14) and (14') are formed, a Cr/Cu/Au layer is mounted during a chip pad metallizing process, a Pb/Sn alloy is coated and then the temperature is heated and it is formed over each of the aforementioned pads (13) and (13').

12. The laminated semiconductor package manufacturing method consisting of stage S1, in which polyimide [layers](12) and (12')

are respectively formed at the surface of one side of both the upper and lower side semiconductor chips (11) and (11'),

stage S2, in which each of the solders (14) and (14') is respectively formed over each of the pads (13) and (13') of the aforementioned upper and lower side semiconductor chips (11) and (11'),

stage S3', in which each of the inner leads (15) and (15) is lined up at each solder (14) of the lower side semiconductor chip (11) at both sides of said chip (11),

and stage S4', in which the upper side semiconductor chip (11') is overturned and mounted at the upper face of each of the aforementioned inner leads (15) and (15); these inner leads (15) and (15) and the upper and lower side semiconductor chips (11) and (11') are bonded all at once in a reflow furnace, and then an encapsulating epoxy [resin] is provided.

13. The laminated semiconductor package manufacturing method described in Claim 12, in which the aforementioned inner leads are not lined up at the aforementioned upper side semiconductor chip (11').

14. The laminated semiconductor package manufacturing method described in Claim 12, in which the aforementioned encapsulating epoxy [resin] is provided through injection molding.

* * *